REMARKS

The Official Action mailed April 19, 2005, has been received and its contents carefully noted. This response is filed within three months of the mailing date of the Official Action and therefore is believed to be timely without extension of time. Accordingly, the Applicants respectfully submit that this response is being timely filed.

The Applicants note with appreciation the consideration of the Information Disclosure Statements filed on May 21, 1999, and April 14, 2004.

Claims 1, 3-10, 12-17, 19-23, 25-35 and 37-45 are pending in the present application, of which claims 1, 8, 14, 21, 27 and 33 are independent. Claims 1 and 8 have been amended to better recite the features of the present invention. Also, claims 8, 14, 21, 27 and 33 have been amended to correct a minor grammatical informality. For the reasons set forth in detail below, all claims are believed to be in condition for allowance. Favorable reconsideration is requested.

Paragraph 2 of the Official Action rejects claims 1, 3-6, 8-10, 12, 14-17, 19, 21-23, 25, 27-31, 33-35, 37 and 39-45 as obvious based on the combination of U.S. Patent No. 6,229,513 to Nakano et al. and U.S. Patent No. 5,734,378 to Okada et al. With respect to independent claims 1 and 8, the Applicants respectfully submit that a *prima facie* case of obviousness cannot be maintained against the independent claims of the present application, as amended. With respect to independent claims 14, 21, 27 and 33, the Applicants respectfully traverse the rejection because the Official Action has not made a *prima facie* case of obviousness.

As stated in MPEP §§ 2142-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the

teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

The Official Action asserts that Nakano discloses "a first clock signal D4 ... and a second clock signal D5 ... having a different phase ... and the [first] clock signal D4 is transmitted to a group A of drain drivers 130 and the second clock signal D5 is transmitted to a group B of drain driver[s] 130" (page 2, Paper No. 20050408). Also, the Official Action asserts that Okada discloses "a delay circuit ... for producing a phase difference ... in a second signal (CK') with respect to a phase of a first clock signal (CK)" (Id.).

However, the prior art, either alone or in combination, does not teach or suggest all the features of the independent claims. Independent claims 1 and 8 have been amended to recite that a second signal is input to at least one of a signal line driving circuit and a scanning line driving circuit to which a first signal is input. Independent claim 14 recites that a first signal and a second signal are input to a same shift register circuit. Independent claim 21 recites that a first signal and a second signal are input to a same latch circuit. Independent claims 27 and 33 recite producing a phase difference in a second signal with respect to a phase of a first signal which is input to at least one of a signal line driving circuit and a scanning line driving circuit, where the second signal is input to the at least one of the signal line driving circuit and the scanning line driving circuit. Nakano and Okada, either alone or in combination, do not teach or suggest the above-referenced features of the present invention.

Each of the group A of drain drivers and the group B of drain drivers is an independent circuit. Nakano teaches that "while display data at a frequency of 32.5 MHz may be recognized by the drain drivers, it is difficult for the drain drivers to recognize the clock signal (D3) at a frequency for 65 MHz" (column 2, lines 24-27). Therefore, Nakano appears to teach that drain drivers are divided into groups A and B in order to lower the frequency of clock signals. However, as shown for example in Figure 7, Nakano appears to teach that first clock signal D4 and the second clock signal D5 are input into independent circuits (see also column 9, line 48 to column 10, line 14). Nakano does not teach or suggest that first clock signal D4 and the second clock signal D5 are input to the same circuit.

Therefore, Nakano and Okada do not teach or suggest that a second signal is input to at least one of a signal line driving circuit and a scanning line driving circuit to which a first signal is input; that a first signal and a second signal are input to a same shift register or latch circuit; or producing a phase difference in a second signal with respect to a phase of a first signal which is input to at least one of a signal line driving circuit and a scanning line driving circuit, where the second signal is input to the at least one of the signal line driving circuit and the scanning line driving circuit. Since Nakano and Okada do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained.

Furthermore, there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify Nakano and Okada or to combine reference teachings to achieve the claimed invention. MPEP § 2142 states that the examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. It is respectfully submitted that the Official Action has failed to carry this burden. While the Official Action relies on various teachings of the cited prior art to disclose aspects of the claimed invention and asserts that these aspects could be used together, it is submitted that the Official Action

does not adequately set forth why one of skill in the art would combine the references to achieve the features of the present invention.

The test for obviousness is not whether the references "could have been" combined or modified as asserted in the Official Action, but rather whether the references should have been. As noted in MPEP § 2143.01, "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990) (emphasis in original). Thus, it is respectfully submitted that the standard set forth in the Official Action is improper to support a finding of *prima facie* obviousness.

The Official Action asserts that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the control circuit of Nakano to have a delay circuit for producing a second clock signal having a different phase from the first clock signal as taught by Okada since the high-speed data transfer and sampling can be easily performed" (pages 2-3, Id.). The Applicants respectfully disagree and traverse the above-referenced assertions in the Official Action.

Even if, as asserted in the Official Action, group A of drain drivers and group B of drain drivers are regarded as one drain driver, the Applicants respectfully submit that there is insufficient motivation to combine Nakano and Okada. Nakano discloses that two groups of drain drivers are provided in order to lower the frequency of clock signals as described above. On the other hand, Okada discloses that an upper bit and a lower bit of image data are transmitted via the same transmission line by using a time series data generator including a delay circuit so as to reduce the number of data lines included in the transmission line of a delay circuit. It is not clear why one of ordinary skill in the art who was concerned with "high-speed data transfer and sampling" would not have simply practiced Okada alone. That is, it is not sufficient to merely point out the advantages of two references and assert that it would have been obvious to combine the two references so that you can have both advantages in one device.

Rather, in order to form a *prima facie* case of obviousness, the Official Action must show that the references should have been combined.

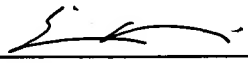
In the present application, it is respectfully submitted that the prior art of record, either alone or in combination, does not expressly or impliedly suggest the claimed invention and the Official Action has not presented a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.

For the reasons stated above, the Official Action has not formed a proper *prima facie* case of obviousness. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) are in order and respectfully requested.

Paragraph 3 of the Official Action rejects dependent claims 7, 13, 20, 26, 32 and 38 as obvious based on the combination of Nakano, Okada and U.S. Patent No. 5,801,678 to Shimada. Shimada does not cure the deficiencies in Nakano and Okada. The Official Action relies on Shimada to allegedly teach the features of the dependent claims. However, Nakano, Okada and Shimada, either alone or in combination, do not teach or suggest that a second signal is input to at least one of a signal line driving circuit and a scanning line driving circuit to which a first signal is input; that a first signal and a second signal are input to a same shift register or latch circuit; or producing a phase difference in a second signal with respect to a phase of a first signal which is input to at least one of a signal line driving circuit and a scanning line driving circuit, where the second signal is input to the at least one of the signal line driving circuit and the scanning line driving circuit. Also, Shimada does not teach or suggest that iw would have been obvious to combine Nakano and Okada. Since Nakano, Okada and Shimada do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) are in order and respectfully requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,



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